Amendments to the Specification:

Page 9, paragraph 19, has been amended as follows:

[19] Driver circuit 10 includes inverters 20 and 22, connected to be driven in parallel by the output of source 12. Driver circuit 10 also comprises output stage 24, including output terminal 26 which is connected in a DC circuit to drive load 14. Output stage 24 is connected to be responsive to output voltages of inverters 20 and 22 via DC ~~circuits~~ paths 28 and 30 which respectively ~~include~~ are shunted by switched voltage controlled shunt capacitors 32 and 34.

Page 9, paragraph 20, has been amended as follows:

[20] Inverter 20 includes complementary transistors in the form of PFET 36 and NFET 38 having gate electrodes connected to be driven in parallel by the bilevel output of source 12 at terminal 39 and source drain paths which are switched on and off in a complementary manner by the voltage applied to the gate electrodes of the PFET and NFET. The source drain paths of PFET 36 and NFET 38 are connected in series with each other and across DC power supply terminals 16 and 18. A resistive impedance, i.e., resistor 40, is connected in series with the source drain paths of PFET 36 and NFET 38, between the drains of the PFET and NFET of inverter 20. The use of resistor 40 as a resistive impedance, is advantageous because it (1) enables a lower resistance to be achieved and (2) provides better resistance value stability with regard to variations of integrated circuit temperature and power supply voltage, and integrated circuit manufacturing. A first end of DC ~~circuit~~ path 28 is connected to a common terminal at one side of resistor 40 and the drain electrode of PFET 36.

Page 10, paragraph 21, has been amended as follows:

[21] Inverter 22 is similar to inverter 20, in that inverter 22 includes PFET 42 and NFET 44 and a resistive impedance in the form of resistor 46. The gate electrodes of PFET 42 and NFET 44 are connected to be driven in parallel by the output voltage of source 12 at terminal 39 and the source drain paths of PFET 42 and NFET 44 are connected in series with each other and a resistive impedance, i.e., resistor 46. However, inverter 22 differs from inverter 20 because the common terminal of resistor 46 and the drain of NFET 44 are connected to a first end of DC ~~circuit~~ path 30. Inverters 20 and 22 thus can be considered as switching circuits for selectively supplying, to the output terminals thereof, voltages substantially equal to the power supply voltages 1.0Vdd and 0Vdd.

Page 10, paragraph 22, has been amended as follows:

[22] Output stage 24 includes PFET 48 and NFET 50 having source drain paths connected in series with each other across DC power supply terminals 16 and 18. The drain electrodes of PFET 48 and NFET 50 have a common connection to output terminal 26 which is connected to load 14. PFET 48 and NFET 50 have gate electrodes respectively connected to the second ends of DC ~~circuits~~ paths 28 and 30. The gate electrodes of PFET 48 and NFET 50 are respectively connected to first electrodes of shunt capacitors 32 and 34. The second electrode of capacitor 32 is connected to ground DC power supply terminal 18, while the second electrode of capacitor 34 is connected to +Vdd power supply terminal 16. Because of the connections of the electrodes of capacitors 32 and 34 to the gate electrodes of PFET 48 and NFET 50 and to the constant voltages at the power supply terminals 16 and 18, the waveforms across the capacitors are independent of the current that load 14 draws from output stage 24. PFET 48 and NFET 50 have thresholds

such that (1) in response to the voltage applied to the gate electrode of PFET 48 being less than and greater than the threshold voltage of the PFET, the PFET source drain path is turned on and off, respectively, and (2) in response to the voltage applied to the gate electrode of NFET 48 being less than and greater than the threshold voltage of the NFET, the NFET source drain path is turned off and on, respectively.

Page 12, paragraph 26, has been amended as follows:

[26] During the half cycles of source 12 when the output voltage of the source has a value of 1.0Vdd, NFETs 38 and 44 are turned on and PFETs 36 and 42 are turned off. Consequently, a voltage approximately equal to the ground voltage at terminal 18 is supplied to the first end of DC ~~circuit~~ path 28 (at the drain of PFET 36) through the low impedance, turned on source drain path of PFET 38 and resistor 40. At the same time, the ground voltage at terminal 18 is supplied to the first, input end of DC ~~circuit~~ path 30 (at the drain of NFET 44) through the low impedance, turned on source drain path of NFET 44. Just before the end of the half cycles when the output voltage of source 12 has a value of 1.0Vdd, inverters 20 and 22 apply low voltages, substantially equal to the voltage at ground terminal 18, to the gate electrodes of PFET 48 and NFET 50, causing the PFET and NFET to be respectively turned on and off. In addition, at this time there is virtually no voltage across the insulator of NFET 52 because the gate electrode thereof and the source drain path thereof are both substantially at ground potential, resulting in the voltage across capacitor 32 being zero. In contrast, because (1) NFET 44 is turned on, causing the input of DC path 30 to be substantially at ground, i.e., 0Vdd, and (2) the source drain path of PFET 54 is at 1.0Vdd, there is a voltage substantially equal to 1.0Vdd across the insulator of PFET 54 that comprises capacitor 34.

Page 13, paragraph 27, has been amended as follows:

[27] During the half cycles of source 12 when the output voltage of the source has a value of 0Vdd, NFETs 38 and 44 are turned off and PFETs 36 and 42 are turned on. Consequently, the 1.0Vdd voltage at terminal 16 is supplied to the first, input end of DC ~~circuit~~ path 28 (at the drain of PFET 36) through the low impedance, turned on source drain path of PFET 36. At the same time, the 1.0Vdd voltage at terminal 16 is supplied to the first end of DC ~~circuit~~ path 30 (at the drain of NFET 44) through resistor 46 and the low impedance, turned on source drain path of PFET 42. Just before the end of the half cycles when the output voltage of source 12 has a value of 0Vdd, inverters 20 and 22 apply high voltages, substantially equal to the 1.0Vdd voltage at power supply terminal 16, to the gate electrodes of PFET 48 and NFET 50, causing the PFET and NFET to be respectively turned off and on. Also, at this time there is virtually no voltage across the insulator of PFET 54 because the gate electrode thereof and the source drain path thereof are both substantially at 1.0Vdd, resulting in the voltage across capacitor 34 being zero. In contrast, because (1) PFET 36 is turned on, causing the input of DC path 28 to be substantially at 1.0Vdd, and (2) the source drain path of NFET 52 is at ground potential, there is a voltage substantially equal to 1.0Vdd across the insulator of NFET 52, which has a finite capacitance value.

Page 14, paragraph 29, has been amended as follows:

[29] At the beginning of and during short duration negative going transitions 68 of the voltage of source 12, from 1.0Vdd to 0Vdd, as indicated by waveform 60, PFET 36 rapidly goes from an off to an on condition while NFET 38 rapidly goes from an on to an off condition. In response to

transitions 68, the voltage at the drain of PFET 36, at the input of DC ~~circuit~~ path 28, changes rapidly in the positive direction, so that the voltage applied to the gate of PFET 48, indicated by waveform 69, changes rapidly, as indicated by waveform portion 70, from a value substantially equal to 0Vdd to a value substantially equal to 1.0Vdd. This results in PFET 48 changing rapidly from an on condition to an off condition, as indicated by the negative going transitions at the ends of intervals 64 of waveform 62, but has no immediate effect on the zero voltage across discharged capacitor 32.